METHOD AND APPARATUS FOR CORRECTING THE PHASE OF A CLOCK IN A DATA RECEIVER

Abstract

A method for correcting the phase of a clock in a data receiver which receives a data flow representing different signal levels with logical high and low signal values and signal transitions positioned therebetween, wherein the positions of such signal transitions between respective two adjacent logical signal values are evaluated for correcting the phase of the clock. The position of a signal transition between a first pair of signal values on one level (11) or a second pair of signal values on the other level (00) is weighted stronger in the evaluation then the positions of signal transitions between adjacent single signal values (1,0) of different signal levels.